transistor 642 is held at the stand-by level, and regulation is performed by primary voltage regulator 610. Positive going dynamic variations in Vout due to a rapid decrease in the current demanded by the load that is beyond the bandwidth of amplifier 646 are regulated by transistor 642. Dynamic regulation is accomplished because the base voltage of transistor 642 established by amplifier 646 lags the transient variation of Vout under this condition. For transistor 642 comprising a bipolar transistor, the output current sourced by transistor 642 from the load is exponentially related to the dynamic change in transistor 642 base-emitter voltage, i.e., I.sub.E.congruent.k.sub.1e.sup.(Vbe/Vt), where k.sub.1 and Vt are constants, I.sub.E is the emitter current of transistor 642 and Vbe is the base-emitter voltage of transistor 642. Voltage peak in the power supply under this dynamic condition is thus reduced. The bandwidth of amplifier ~~642~~ 646 is selected based on factors such as dynamic response of primary voltage regulator 610, secondary voltage regulator components, e.g., positive transient regulator 640, the desired degree of high frequency voltage regulation, and the efficiency of power delivery system 600.

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Please amend page 16, lines 5-~~15~~ 12 of the application as follows:

As the load current (I_Load) rapidly transitions from a high current (I_high) to a low current (I_low) beginning at time t4 at such a rate that primary voltage regulator 1 110 cannot immediately respond to the change in load current, the voltage at the load element (V_Load) rapidly transitions from a desirable nominal voltage (V_nom) to an undesirable voltage (V_nom+V_spike) as the dynamic load charge is momentarily absorbed by capacitive storage lo elements in close proximity to the load. Between time t5 and t6, the local capacitive storage

elements absorb the charge provided by the primary regulator that is no longer demanded by the load 1140, resulting in an undesirable boost in the load voltage (V_Load).

Please amend page 16, lines 17 - page 17, line 7 of the application as follows:

Typical current waveforms of system 1100 in accordance with one embodiment of the invention are illustrated in Figure 13 and serve to further illustrate the operation of the improved regulation system. First, consider the condition whereby the load current (I_Load) rapidly transitions from a low current state (I_low) to a high current state (I_high) beginning at time t0 at such a rate that primary voltage regulator 1110 cannot immediately source the demanded charge. Secondary regulator 1120 then responds at time t1 and rapidly provides the demanded increase in load current (*e.g.* using Iboost1 1150 and circuit 1180) as shown by the I_SR waveform of Figure 13. Secondary regulator 1120 is preferably designed in such a way as to minimize the time between t0 and t1. The rapid delivery of dynamic charge to the load by secondary regulator 1120 results in a significant improvement in the dynamic regulation accuracy of the voltage supplied to load 1140 (V_Load) such that the dynamic perturbation is reduced to V_nom-V_reg where V_reg is << ~~than~~ V_spike of Figure 12. Secondary regulator 1120 continues to provide the demanded load current until such time that primary voltage regulator 1110 can respond which begins at time t2 thereby maintaining the desired nominal load voltage (V_nom). In accordance with the illustrated embodiment, during the transition period between time t2 and t3, secondary regulator 1120 output current response is designed to approximately inversely match the response of primary voltage regulator 1110 (I_PR) for maximum regulation accuracy i.e. the sum of the current provided by primary regulator 1110 (I_PR) and secondary regulator 1120

(I_SR) approximately equals load element 1140 current (I_Load). Overall efficiency is maximized when secondary regulator 1120 output current hold time (t2-t1) and transition time (t3-t2) is minimized.

Please amend page 19, line 23- page 20 line 10 of the application as follows:

Secondary regulator 1520 also contains a sense amplifier 1536, a boost transistor 1538, diodes ~~1540~~ 1541 and 1542, a controlled current source 1543 having an output current of Iboost1, and a circuit 1544 to control the current source. Initially, Iboost1 is zero, diodes ~~1540~~ 1541 and 1542 are not conducting current, and transistor 1538 is reversed biased and not conducting current. Sense amplifier 1536 sense at a load point 1546 and produces an output signal whose magnitude is in proportion to or otherwise related to the rate of change of the load current, thereby allowing secondary regulator 1520 to distinguish between load transient events that can be regulated by primary voltage regulator 1510 and transient events that require secondary regulator 1520 to respond for maximum overall system 1500 regulation effectiveness and efficiency. For low to high current load transients, circuit 1544 translates sense amplifier 1536 output into a signal suitable for control of source 1543 which is modulated from a zero or near zero state to an active or "on" state. In response to the current from source 1543, diodes ~~1540~~ 1541 and 1542 conduct current, transistor 1538 is forward biased and conducting current, and transistor 1522 conducts current in proportion to Iboost1 and the emitter area ratio of transistor 1538, diode ~~1540~~ 1541 and 1542 and transistor 1522. Transistor 1522 then becomes an active charge-sourcing element and responds to satisfy the demand in load current. Charge is then quickly transferred from a secondary output voltage node 1115 to primary voltage node